Descriptions

This -30V -4.2A P-Channel Enhancement Mode field effect transistor in a SOT-23 plastic package.

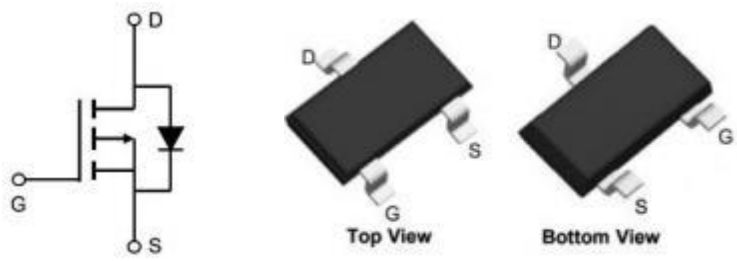
Features

- Advanced Trench Process Technology
- Fast Switching Speed
- Low Threshold Voltage
- Halogen-Free & Lead-Free

Applications

- Load Switch for Portable Devices
- Voltage controlled small signal switch

Equivalent Circuit & Pinning



Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient 3)	$R_{\theta JA}$	100	℃/W

Note：
1 ）Pulse width ≤100us, duty cycle ≤1%,limite by Tjmax.
2）Device mounted on FR-4 substrate PC board, 2ozcopper, with 1-inch square copper plate in still air.

Absolute Maximum Ratings(Ta=25℃)

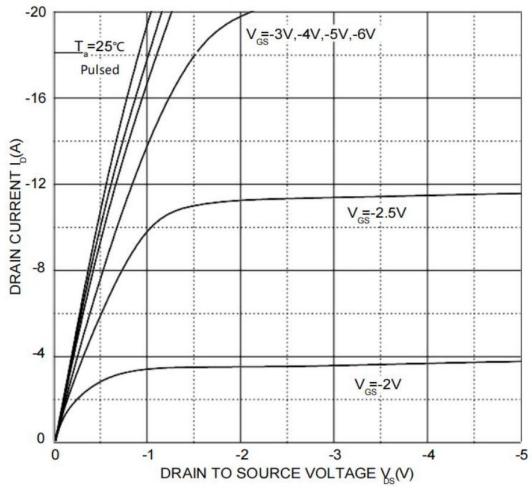
Parameter	Symbol	Value	Unit
Drain- Source Voltage	V_{DS}	-30	V
Gate- Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	-4.2	A
Peak Drain Current, Pulsed 1) V_{GS}= 10V	I_{DM}	-25	A
Power Dissipation Tc = 25℃	P_{tot}	1.25	W
Operating Junction and Storage Temperature Range	T_J , T_{stg}	-55~ 150	℃

Electrical Characteristics(Ta=25℃)

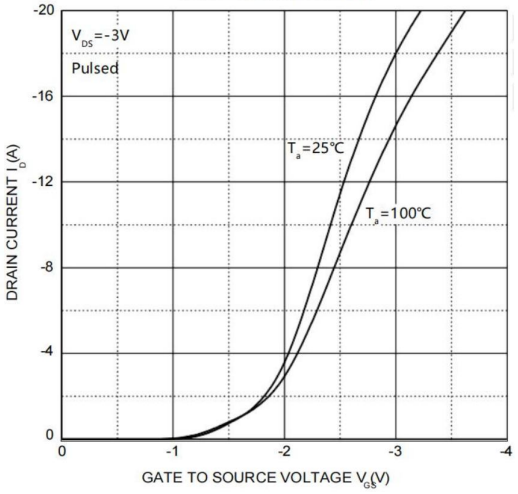
Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain- Source Breakdown Voltage at I_D = -250 μA	BV_{DSS}	-30			V
Drain- Source Leakage Current at V_{DS} = -24 V	I_{DSS}			- 1	μA
Gate Leakage Current at V_{GS} = ± 12V	I_{GSS}			±100	nA
Gate- Source Threshold Voltage at V_{DS} = V_{GS}, I_D =- 250 μA	$V_{GS(th)}$	-0.7		- 1.3	V
Drain- Source On- State Resistance at V_{GS} = -10 V, I_D = -2 A at V_{GS} = -4 .5 V, I_D = -2 A	$R_{DS(on)}$		41 48	60 70	mΩ
DYNAMIC PARAMETERS					
Input Capacitance at V_{DS} = -5 V , I_D = -5A	gfs	7			S
Gate resistance at V_{DS} = 0 V , f = 1 MHz	Rg		1.8		Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = - 15 V, f = 1 MHz	C_{iss}		1050		pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = - 15 V, f = 1 MHz	C_{oss}		127		pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = - 15 V, f = 1 MHz	C_{rss}		85		pF
Gate charge total at V_{DS} =- 15 V, I_D =- 5.5 A, V_{GS} =- 10 V	Q_g		12		nC
Gate to Source Charge at V_{DS} =- 15 V, I_D =- 5.5 A, V_{GS} =- 10 V	Q_{gs}		3.		nC
Gate to Drain Charge at V_{DS} =- 15 V, I_D =- 5.5 A, V_{GS} =- 10 V	Q_{gd}		3		nC
Turn-On Delay Time at V_{GS}= - 10 V, V_{DS} = - 1.5 V, R_L=3 .6Ω , R_{GEN} = 6 Ω	$t_{d(on)}$		6.5		ns
Turn-On Rise Time at V_{GS}= - 10 V, V_{DS} = - 1.5 V, R_L=3 .6Ω , R_{GEN} = 6 Ω	t_r		3.5		ns
Turn-Off Delay Time at V_{GS}= - 10 V, V_{DS} = - 1.5 V, R_L=3 .6Ω , R_{GEN} = 6 Ω	$t_{d(off)}$		140		ns
Turn-Off Fall Time at V_{GS}= - 10 V, V_{DS} = - 1.5 V, R_L=3 .6Ω , R_{GEN} = 6 Ω	t_f		13		ns
Body- Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = -2 A, V_{GS} = 0 V	V_{SD}			- 1	V

Electrical Characteristic Curve

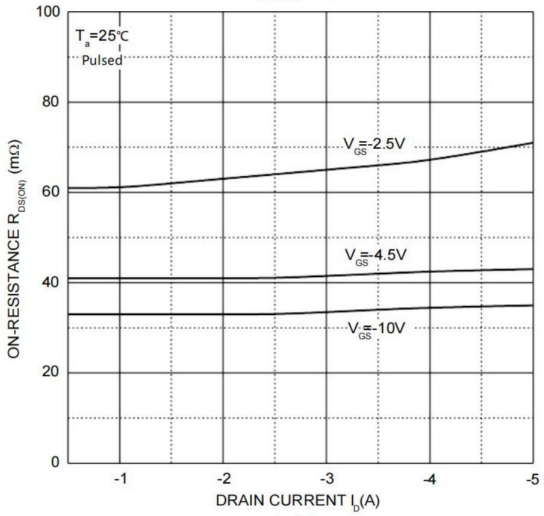
Output Characteristics



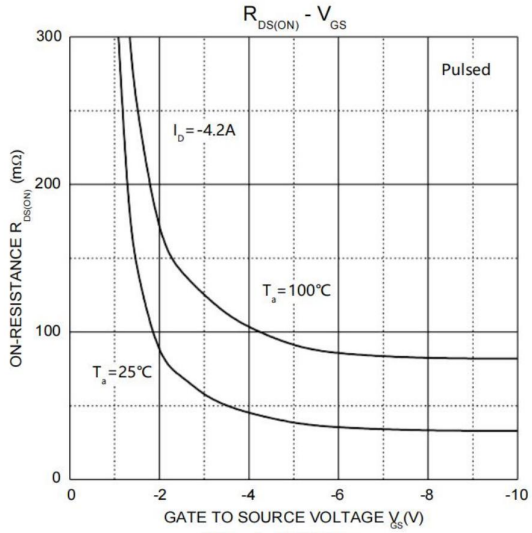
Transfer Characteristics



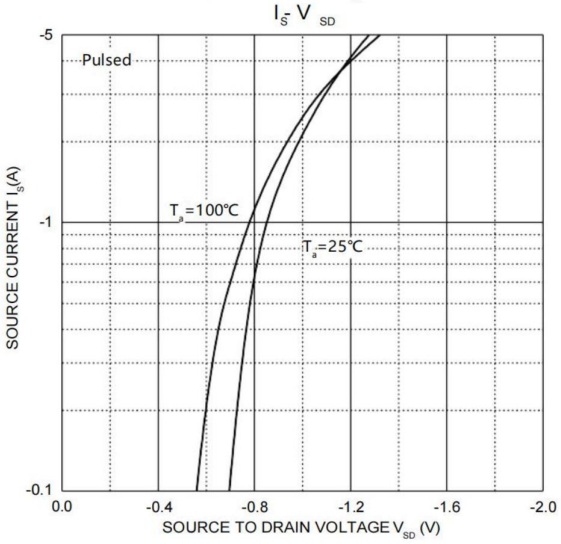
$R_{DS(ON)}$ – I_D



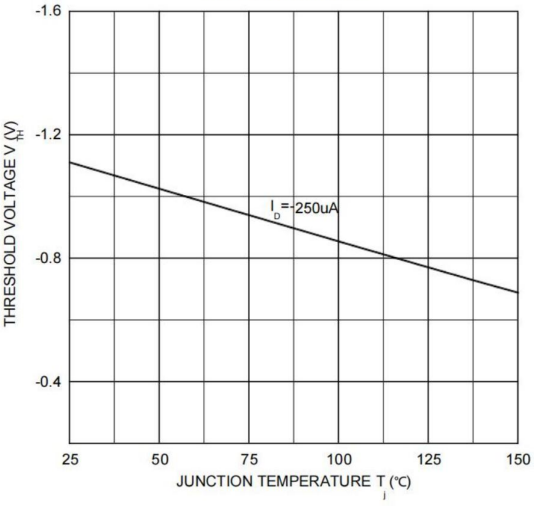
$R_{DS(ON)}$ - V_{GS}



I_S- V_{SD}



Threshold Voltage



Test Circuits

Fig. 1- 1 Switching times test circuit

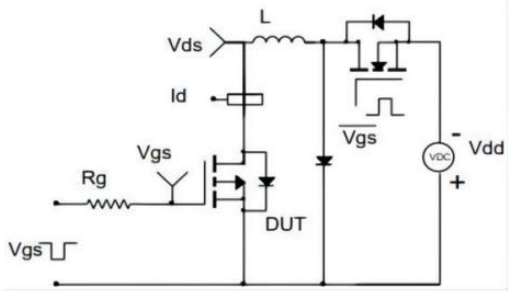


Fig. 1-2 Switching Waveform

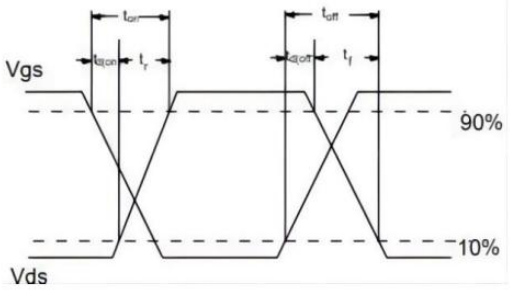


Fig.2- 1 Gate charge test circuit

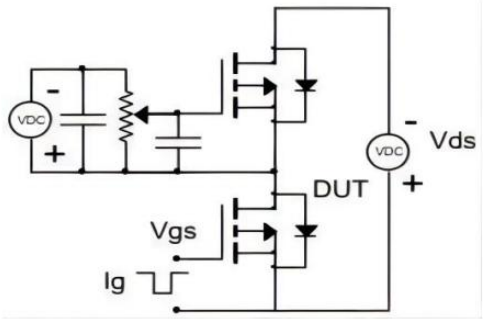


Fig.2-2 Gate charge waveform

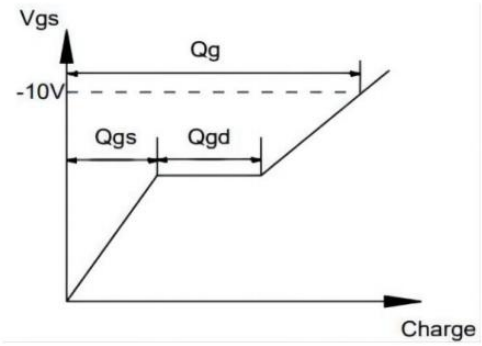


Fig.3- 1 Avalanche test circuit

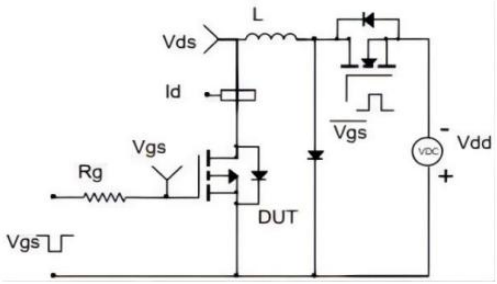
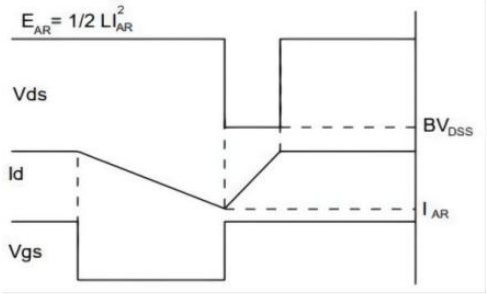
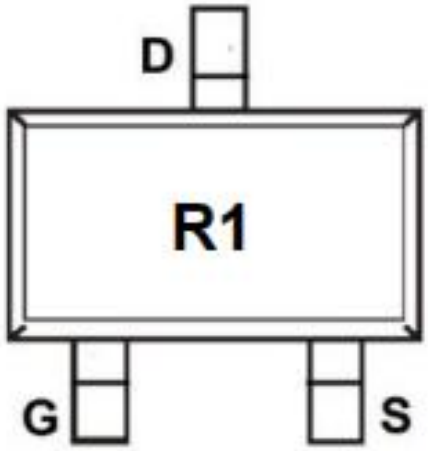


Fig.3-2 Avalanche waveform

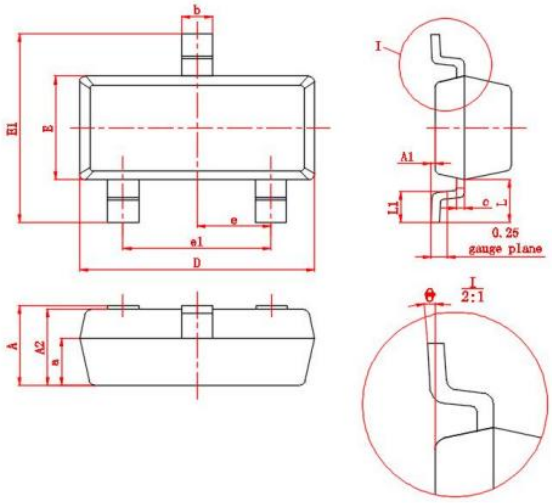


Marking Instructions



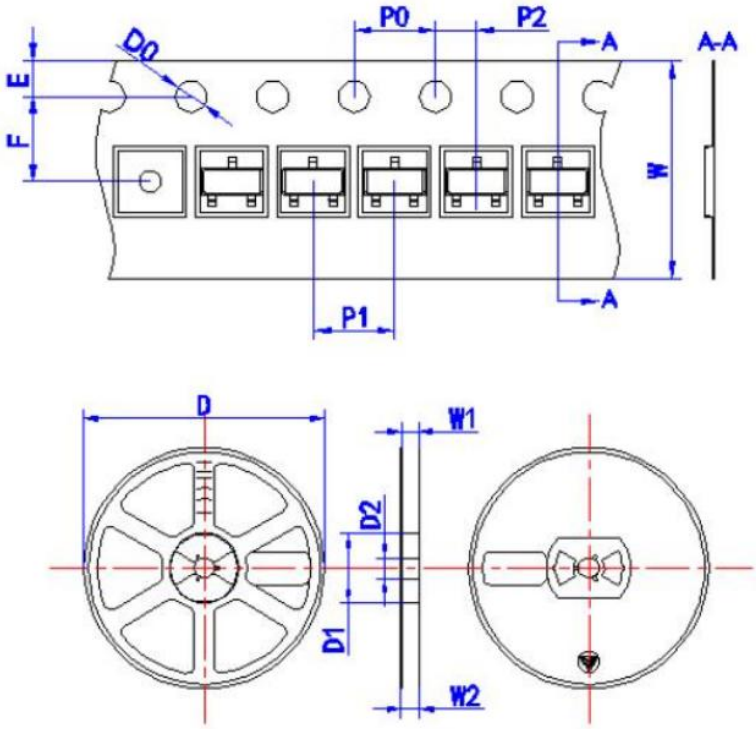
Marking: R1

Package Outline Dimensions



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
A	0.9	1.15	E	1.2	1.4	c	0.08	0.15
A1	0	0.1	E1	2.25	2.55	L	(0.55)	
A2	0.9	1.05	e	(0.95)		L1	0.3	0.5
a	(0.6)		e1	1.8	2.0	θ	0°	8°
D	2.8	3.0	b	0.3	0.5			

Emboss Carrier Tape&Reel



Symbol	Dimension in Millimeters
Tape	
D0	1.50+0.10/-0.00
E	1.75±0.10
F	3.50±0.10
P0	4.00±0.10
P1	4.00±0.10
P2	2.00±0.10
W	8.00+0.3/-0.1
Reel	
D	178.0±2.00
D1	54.40±1.00
D2	13.00±1.00
W1	9.50±1.00
W2	12.30±1.00